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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/748,758	MORROW ET AL.	
	Examiner	Art Unit	
	PHYOWAI LIN	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *23 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :10/17/2007,11/30/2007 and 03/07/2008.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US Pub Number 2004/0144994) in view of Findakly et al. (US Patent Number 6504961).

Regarding to claims 1, Lee et al. teach an apparatus (see FIGs.3 and 10-11), comprising:

an integrated circuit (controller 850) to communicate with a memory (memory device 840), the integrated circuit having an optical transmitter (communication unit 852) (see paragraph [0042] lines 1-4; paragraph [0041] lines 20-21 and FIG.10);

an optical bus (optical path 853) coupled to the optical transmitter (see paragraph [0042] lines 1-4 and FIG.10);

N optical receivers (T/R units 848) coupled to the optical bus via N optical couplers (beam splitters 870a-870d) (see paragraph [0041] lines 3-8; paragraph [0042] lines 8-14 and FIG.10 where in T/R units 848 are coupled to the optical path 853 through beam splitter 870a-870d);

N memory modules (memory modules 844a-844d) coupled to the N optical receivers (T/R units 848) (see FIG.10 where in T/R units 848 are coupled to the memory modules 844a-844d); and

one or more memory devices (memory devices 840) coupled to the N memory modules (see column [0041] lines 20-21 and FIG.10);

the optical bus to propagate the optical signal, each of the N optical couplers to couple one-Nth of the power of the optical signal from the optical bus to its associated optical receiver, each optical receiver to convert its one-Nth of the optical signal to second set of electrical signals, the N memory modules to couple the second set of electrical signals to the memory devices. (see paragraph [0041] lines 3-8; paragraph [0042] lines 8-14; paragraph [0041] lines 20-22 and FIG.10-11 where in first portion 876 of the optical power signal 874 from the optical bus are coupled into the first T/R unit 848 through first beam splitter 870a and the first portion 876 of the optical power signal accesses with the memory device 840, a second portion 878 of the optical power signal 874 from the optical bus are passed to the second T/R unit 848 through second beam splitter 870b and the second portion 878 of the optical power signal accesses with the memory device 840 and so on to the third T/R unit 848 and fourth T/R unit 848 as well).

Lee et al.'s apparatus in FIG.10-11 do not specifically teach the optical transmitter to convert a signal to communicate with the memory devices from a first electrical signal to an optical signal; the optical bus to propagate the one-Nth (equal) power of the optical signal from the optical bus to its associated optical receiver and

power of the optical signal from the receiver (T/R 848) converts to second set of electrical signals to the memory devices.

However, Lee et al.'s apparatus in FIG.3 teaches the optical transmitter (communication unit 152) to convert a signal to communicate with the memory devices (memory devices 140) from a first electrical signal to an optical signal (see paragraph [0024] lines 8-12; paragraph [0023] lines 1-4 and FIG.3 where in the communication unit 152 converts the electrical signals from the bus bridge 16 into the optical signals for communicating with the memory devices 140) and the power of the optical signal from the receiver converts to second set of electrical signals to the memory devices (see paragraph [0025] lines 1-10 and FIG.3).

Findakly et al. disclose the system having 1x8 coupler 118 which utilize the reflectances of the partial reflectors 102, 104, 106, 108, 110, 112, 114 and 116 in order to provide equal optical light intensity to each of the output fibers 84,86, 88, 90, 92, 94, 96 and 98 (see column 4,lines 30-32; claim 2 and FIG.2).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to combine Lee et al.'s apparatus in FIG.10-11 with the teachings of Lee et al.'s apparatus in FIG.3 and Findakly for sending the electrical signal from the bus bridge 16 to the communication unit 852 for communicating with the memory devices in electrical form and implementing the characteristics of reflectances of the partial reflectors in the beam splitters 870a-d of Lee et al. through the common optical bus because it would allow the system memory 820 receiving a memory request signal from the external device (e.g. CPU device) through the bus bridge 16 and using

control signal to determine which memory module corresponding to the memory request signal, receiving the equal amount of optical power signal at the associated optical receiver and reducing the fiber connection cost from receiver to the memory devices by using electrical connection.

Regarding to claim 2, Lee et al. and Findakly et al. disclose everything claimed as applied above (see claim 1). In addition, Lee et al. disclose the apparatus further includes: wherein the integrated circuit is a memory controller (controller 850) (see paragraph [0042] lines 1-4 and FIG.10).

Regarding to claim 3, Lee et al. and Findakly et al. disclose everything claimed as applied above (see claim 1). In addition, Lee et al. disclose the apparatus further includes: wherein the integrated circuit is a processor (see paragraph [0042] lines 1-4 and FIG.10 where in a processor inherently exists inside the controller 850).

Regarding to claim 4, Lee et al. and Findakly et al. disclose everything claimed as applied above (see claim 1). In addition, Lee et al. disclose the apparatus further includes: wherein the optical bus includes at least optical fiber (see paragraph [0042] lines 1-4 and FIG.10 where in the optical fiber inherently exists along the optical path 853).

Regarding to claim 5, Lee et al. and Findakly et al. disclose everything claimed as applied above (see claim 1). In addition, Lee et al. disclose the apparatus further includes: wherein the optical transmitter includes a laser (see paragraph [0042] lines 1-4 and FIG.10 where in a laser source inherently exists inside communication unit 852).

Regarding to claims 6 and 7, Lee et al. and Findakly et al. disclose everything claimed as applied above (see claim 1). In addition, Lee et al. disclose the apparatus further includes: wherein the couplers are directional couplers which include an optical fiber (see paragraph [0041] lines 3-8; paragraph [0042] lines 1-4; paragraph [0042] lines 8-10 and FIG.10-11 where in the beam splitters 870a-870d are coupled with optical path 853 and direct the portion of optical signal to the T/R units 848 as directional couplers).

Regarding to claims 8 and 9, Lee et al. and Findakly et al. disclose everything claimed as applied above (see claim 1). In addition, Lee et al. disclose the apparatus further includes: where in the couplers are free space couplers as well as beam splitters (beam splitter 870a-870d) (see paragraph [0042] lines 1-4 and FIG.10-11).

Regarding to claim 10, Lee et al. disclose an article of manufacture, comprising a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the operations (see FIGs.3 and 10-11) comprising:

propagating the optical signal on an optical bus (optical path 853) to N optical couplers (beam splitters 870a-870d) (see paragraph [0042] lines 1-4 and FIG.10-11 where in the communication unit 852 transmits an optical signal to the beam splitters 870a-870d);

coupling one-Nth of the power of the optical signal from the optical bus to each one of N optical receivers (T/R units 848) (see paragraph [0041] lines 3-8; paragraph [0042] lines 8-14 and FIG.10-11 where in first portion 876 of the optical power signal 874 from the optical bus are coupled into the first T/R unit 848 through first beam splitter

870a, a second portion 878 of the optical power signal 874 from the optical bus are passed to the second T/R unit 848 through second beam splitter 870b and so on to the third T/R unit 848 and fourth T/R unit 848 as well);

each optical receiver converting its one-Nth of the optical signal to a second set of electrical signals; and coupling the second set of electrical signals to one or more memory devices via N memory modules (see paragraph [0041] lines 3-8; paragraph [0042] lines 8-14; paragraph [0041] lines 20-22 and FIG.10-11 where in first portion 876 of the optical power signal 874 from the optical bus are coupled into the first T/R unit 848 through first beam splitter 870a and the first portion 876 of the optical power signal accesses with the memory device 840, a second portion 878 of the optical power signal 874 from the optical bus are passed to the second T/R unit 848 through second beam splitter 870b and the second portion 878 of the optical power signal accesses with the memory device 840 and so on to the third T/R unit 848 and fourth T/R unit 848 as well).

Lee et al.'s apparatus in FIG.10-11 do not specifically teach the optical transmitter to convert a signal to communicate with the memory devices from a first electrical signal to an optical signal; the optical bus to propagate the one-Nth (equal) power of the optical signal from the optical bus to its associated optical receiver and power of the optical signal from the receiver (T/R 848) converts to second set of electrical signals to the memory devices.

However, Lee et al.'s apparatus in FIG.3 teaches the optical transmitter (communication unit 152) to convert a signal to communicate with the memory devices (memory devices 140) from a first electrical signal to an optical signal (see paragraph

[0024] lines 8-12; paragraph [0023] lines 1-4 and FIG.3 where in the communication unit 152 converts the electrical signals from the bus bridge 16 into the optical signals for communicating with the memory devices 140) and the power of the optical signal from the receiver converts to second set of electrical signals to the memory devices (see paragraph [0025] lines 1-10 and FIG.3).

Findakly et al. disclose the system having 1x8 coupler 118 which utilize the reflectances of the partial reflectors 102, 104, 106, 108, 110, 112, 114 and 116 in order to provide equal optical light intensity to each of the output fibers 84,86, 88, 90, 92, 94, 96 and 98 (see column 4,lines 30-32; claim 2 and FIG.2).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to combine Lee et al.'s apparatus in FIG.10-11 with the teachings of Lee et al.'s apparatus in FIG.3 and Findakly et al. for sending the electrical signal from the bus bridge 16 to the communication unit 852 for communicating with the memory devices in electrical form and implementing the characteristics of reflectances of the partial reflectors in the beam splitters 870a-d of Lee et al. through the common optical bus because it would allow the system memory 820 receiving a memory request signal from the external device (e.g. CPU device) through the bus bridge 16 and using control signal to determine which memory module corresponding to the memory request signal, receiving the equal amount of optical power signal at the associated optical receiver and reducing the fiber connection cost from receiver to the memory devices by using electrical connection.

Regarding to claim 11, Lee et al. and Findakly et al. disclose everything claimed as applied above (see claim 10). In addition, Lee et al. disclose the apparatus further includes: wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising propagating the optical signal on a waveguide or optical fiber (see paragraph [0042] lines 1-4 and FIG.10).

Regarding to claim 12, Lee et al. and Findakly et al. disclose everything claimed as applied above (see claim 11). In addition, Lee et al. disclose the apparatus further includes: wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising coupling one-Nth of the optical signal from the optical bus to each one of N optical receivers via a directional coupler (beam splitter 870a) (see paragraph [0041] lines 3-8; paragraph [0042] lines 8-14; paragraph [0041] lines 20-22 and FIG.10-11 where in first portion 876 of the optical power signal 874 from the optical bus are coupled into the first T/R unit 848 through first beam splitter 870a).

Regarding to claim 13, Lee et al. and Findakly et al. disclose everything claimed as applied above (see claim 10). In addition, Lee et al. disclose the apparatus further includes: wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising propagating the optical signal via free space (see FIG.10 where in the optical signals propagate along the optical path 853 to each memory module 844 thorough free space).

Regarding to claim 14, Lee et al. and Findakly et al. disclose everything claimed as applied above (see claim 11). In addition, Lee et al. disclose the apparatus further includes: wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising coupling one-Nth of the optical signal from the optical bus to each one of N optical receivers via a directional coupler (beam splitter 870a) (see paragraph [0041] lines 3-8; paragraph [0042] lines 8-14; paragraph [0041] lines 20-22 and FIG.10-11 where in first portion 876 of the optical power signal 874 from the optical bus are coupled into the first T/R unit 848 through first beam splitter 870a).

Regarding to claim 15, Lee et al. disclose an apparatus (see FIGs.3 and 10-11), comprising:

one or more memory devices (memory devices 840) to communicate with an integrated circuit (controller 850), the integrated circuit having an optical receiver (optical receiver inherently exists inside communication unit 852) (see paragraph [0042] lines 16-28 and FIGs 10-11);

N memory modules (memory modules 844a-844d) coupled to the memory devices (memory devices 840) (see FIG.10 where in each memory module 844 couples to the memory devices 840);

N optical transmitters (T/R units 848) coupled to the N memory modules (memory modules 844a-844d) (see paragraph [0042] lines 16-28 and FIGs 10-11); and

an optical bus (optical path 853) coupled to the optical receiver (see paragraph [0042] lines 16-28 and FIGs 10-11where in the optical path 853 couples to the communication unit 852 which has the optical receiver init) ,

each of the N optical transmitters to convert a signal to communicate with the integrated circuit from an electrical signal to an optical signal (see paragraph [0042] lines 14-28 and FIG.s10-11 where in T/R units 848 receive the responsive optical signal 877 and 879 from the memory devices 840 and transmit back to the controller 850), the optical bus to propagate the optical signals to the optical receiver, the optical receiver to convert one –Nth of the power of the optical signals to electrical signals (see FIG.10 where in the optical path 853 couples to the communication unit 852 which has the optical receiver init and optical receiver which has photodetectorfor converting incoming optical signals from the optical bus to electrical signals).

Lee et al.'s apparatus in FIG.10-11 do not specifically teach how electrical signal from the memory devices 840 converts to the optical signal that couples to the T/R unit 848 for communicating with the controller 850 and the optical bus to propagate the one-Nth (equal) power of the optical signal from the optical bus to its associated optical receiver.

However, Lee et al.'s apparatus in FIG.3 teaches using a converter that converts the electrical signal from the memory devices to the optical signals which couples to the T/R unit 148 for communicating with the controller 150 (see paragraph [0025] lines 10-14 and FIG.3).

Findakly et al. disclose the system having 1x8 coupler 118 which utilize the reflectances of the partial reflectors 102, 104, 106, 108, 110, 112, 114 and 116 in order to provide equal optical light intensity to each of the output fibers 84,86, 88, 90, 92, 94, 96 and 98 (see column 4,lines 30-32; claim 2 and FIG.2).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to combine Lee et al.'s apparatus in FIG.10-11 with the teachings of Lee et al.'s apparatus in FIG.3 and Findakly for using a converter that converts the electrical response signals from the memory devices to the optical signals which couples to the T/R unit 148 for communicating with the controller and implementing the characteristics of reflectances of the partial reflectors in the beam splitters 870a-d of Lee et al. through the common optical bus because it would allow the system memory achieving fewer signal power loss along the optical path to the memory controller by applying optical communication technique and receiving the equal amount of optical power signal at the associated optical receiver

Regarding to claim 16, Lee et al. and Findakly et al. disclose everything claimed as applied above (see claim 15). In addition, Lee et al. disclose the apparatus further includes: wherein the integrated circuit is a memory controller (controller 850) (see paragraph [0042] lines 1-4 and FIG.10).

Regarding to claim 17, Lee et al. and Findakly et al. disclose everything claimed as applied above (see claim 15). In addition, Lee et al. disclose the apparatus further

includes: wherein the integrated circuit is a processor (see paragraph [0042] lines 1-4 and FIG.10 where in a processor inherently exists inside the controller 850).

Regarding to claim 18, Lee et al. and Findakly et al. disclose everything claimed as applied above (see claim 15). In addition, Lee et al. disclose the apparatus further includes: wherein the optical bus includes at least optical fiber (see paragraph [0042] lines 1-4 and FIG.10 where in the optical fiber inherently exists along the optical path 853).

Regarding to claim 19, Lee et al. and Findakly et al. disclose everything claimed as applied above (see claim 15). In addition, Lee et al. disclose the apparatus further includes: wherein the optical receiver includes a photodetector (see paragraph [0042] lines 16-28 and FIGs 10-11 where in optical receiver wit photodiode inherently exists inside communication unit 852 for receiving response signal from the memory devices 840).

Regarding to claims 20 and 21, Lee et al. and Findakly et al. disclose everything claimed as applied above (see claim 1). In addition, Lee et al. disclose the apparatus further includes: wherein the couplers are directional couplers which include an optical fiber (see paragraph [0041] lines 3-8; paragraph [0042] lines 1-4; paragraph [0042] lines 8-10 and FIG.10-11 where in the beam splitters 870a-870d are coupled with optical path 853 and direct the portion of optical signal to the T/R units 848 as directional couplers).

3. **Claims 22-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US Pub Number 2004/0144994) in view of Moyer (US Patent Number 5638520) and Sheaffer (US Pub Number 2003/0188244).

Regarding to claim 22, Lee et al. disclose a system (see FIGs.3 and 10-11) comprising:

an integrated circuit (controller 850) to communicate with a memory (memory device 840), the integrated circuit having an optical transmitter (communication unit 852) (see paragraph [0042] lines 1-4; paragraph [0041] lines 20-21 and FIG.10);

an optical bus (optical path 853) coupled to the optical transmitter (see paragraph [0042] lines 1-4 and FIG.10);

N optical receivers (T/R units 848) coupled to the optical bus via N optical couplers (beam splitters 870a-870d) (see paragraph [0041] lines 3-8; paragraph [0042] lines 8-14 and FIG.10 where in T/R units 848 are coupled to the optical path 853 through beam splitter 870a-870d);

N memory modules (memory modules 844a-844d) coupled to the N optical receivers (T/R units 848) (see FIG.10 where in T/R units 848 are coupled to the memory modules 844a-844d); and

one or more memory devices (memory devices 840) coupled to the N memory modules (see column [0041] lines 20-21 and FIG.10);

the optical bus to propagate the optical signal, each of the N optical couplers to couple one-Nth of the power of the optical signal from the optical bus to its associated

optical receiver, each optical receiver to convert its one-Nth of the optical signal to second set of electrical signals, the N memory modules to couple the second set of electrical signals to the memory devices. (see paragraph [0041] lines 3-8; paragraph [0042] lines 8-14; paragraph [0041] lines 20-22 and FIG.10-11 where in first portion 876 of the optical power signal 874 from the optical bus are coupled into the first T/R unit 848 through first beam splitter 870a and the first portion 876 of the optical power signal accesses with the memory device 840, a second portion 878 of the optical power signal 874 from the optical bus are passed to the second T/R unit 848 through second beam splitter 870b and the second portion 878 of the optical power signal accesses with the memory device 840 and so on to the third T/R unit 848 and fourth T/R unit 848 as well).

Lee et al.'s apparatus in FIG.10-11 do not specifically teach the optical transmitter to convert a signal to communicate with the memory devices from a first electrical signal to an optical signal; the optical bus to propagate the one-Nth (equal) power of the optical signal from the optical bus to its associated optical receiver and power of the optical signal from the receiver (T/R 848) converts to second set of electrical signals to the memory devices and a graphics controller coupled to the integrated circuit.

However, Lee et al.'s apparatus in FIG.3 teaches the optical transmitter (communication unit 152) to convert a signal to communicate with the memory devices (memory devices 140) from a first electrical signal to an optical signal (see paragraph [0024] lines 8-12; paragraph [0023] lines 1-4 and FIG.3 where in the communication unit 152 converts the electrical signals from the bus bridge 16 into the optical signals for

communicating with the memory devices 140) and the power of the optical signal from the receiver converts to second set of electrical signals to the memory devices (see paragraph [0025] lines 1-10 and FIG.3).

Findakly et al. disclose the system having 1x8 coupler 118 which utilize the reflectances of the partial reflectors 102, 104, 106, 108, 110, 112, 114 and 116 in order to provide equal optical light intensity to each of the output fibers 84,86, 88, 90, 92, 94, 96 and 98 (see column 4,lines 30-32; claim 2 and FIG.2).

Sheaffer discloses a system, which has graphic controller that is coupled to the memory controller with main memory of the integrated circuit chip for controlling the display of information on a suitable display 132 (see paragraph [0026] and FIG.1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to combine Lee et al.'s apparatus in FIG.10-11 with the teachings of Lee et al.'s apparatus in FIG.3, Findakly et al. and Sheaffer for sending the electrical signal from the bus bridge 16 to the communication unit 852 for communicating with the memory devices in electrical form, implementing the characteristics of reflectances of the partial reflectors in the beam splitters 870a-d of Lee et al. through the common optical bus through the common optical bus and implementing graphic controller which connects to the memory controller for controlling the display of information on a display because it would allow the communication unit 852 receiving a memory request signal from the external device (e.g. CPU device) through the bus bridge 16 and using control signal to determine which memory module corresponding to the memory request signal, receiving the equal amount of optical

power signal at the associated optical receiver, reducing the fiber connection cost from receiver to the memory devices by using electrical connection and the optically-coupled memory system having accurate and useful display system for displaying the receiving data signals from the memory devices.

Regarding to claim 23, Lee et al., Findakly et al. and Sheaffer disclose everything claimed as applied above (see claim 22). In addition, Lee et al. disclose the apparatus further includes: wherein the integrated circuit is a memory controller (controller 850) (see paragraph [0042] lines 1-4 and FIG.10).

Regarding to claim 24, Lee et al., Findakly et al. and Sheaffer disclose everything claimed as applied above (see claim 22). In addition, Lee et al. disclose the apparatus further includes: wherein the integrated circuit is a processor (see paragraph [0042] lines 1-4 and FIG.10 where in a processor inherently exists inside the controller 850).

Regarding to claim 25, Lee et al. disclose an apparatus (see FIGs.3 and 10-11), comprising:

one or more memory devices (memory devices 840) to communicate with an integrated circuit (controller 850), the integrated circuit having an optical receiver (optical receiver inherently exists inside communication unit 852) (see paragraph [0042] lines 16-28 and FIGs 10-11);

N memory modules (memory modules 844a-844d) coupled to the memory devices (memory devices 840) (see FIG.10 where in each memory module 844 couples to the memory devices 840);

N optical transmitters (T/R units 848) coupled to the N memory modules (memory modules 844a-844d) (see paragraph [0042] lines 16-28 and FIGs 10-11); and

an optical bus (optical path 853) coupled to the optical receiver (see paragraph [0042] lines 16-28 and FIGs 10-11where in the optical path 853 couples to the communication unit 852 which has the optical receiver init) ,

each of the N optical transmitters to convert a signal to communicate with the integrated circuit from an electrical signal to an optical signal (see paragraph [0042] lines 14-28 and FIG.s10-11 where in T/R units 848 receive the responsive optical signal 877 and 879 from the memory devices 840 and transmit back to the controller 850), the optical bus to propagate the optical signals to the optical receiver, the optical receiver to convert one –Nth of the power of the optical signals to electrical signals (see FIG.10 where in the optical path 853 couples to the communication unit 852 which has the optical receiver init and optical receiver which has photodetectorfor converting incoming optical signals from the optical bus to electrical signals).

Lee et al.'s apparatus in FIG.10-11 do not specifically teach how electrical signal from the memory devices 840 converts to the optical signal that couples to the T/R unit 848 for communicating with the controller 850, the optical bus to propagate the one-Nth (equal) power of the optical signal from the optical bus to its associated optical receiver and a graphics controller coupled to the integrated circuit.

However, Lee et al.'s apparatus in FIG.3 teaches using a converter that converts the electrical signal from the memory devices to the optical signals which couples to the

T/R unit 148 for communicating with the controller 150 (see paragraph [0025] lines 10-14 and FIG.3).

Findakly et al. disclose the system having 1x8 coupler 118 which utilize the reflectances of the partial reflectors 102, 104, 106, 108, 110, 112, 114 and 116 in order to provide equal optical light intensity to each of the output fibers 84,86, 88, 90, 92, 94, 96 and 98 (see column 4,lines 30-32; claim 2 and FIG.2).

Sheaffer discloses a system, which has graphic controller that is coupled to the memory controller with main memory of the integrated circuit chip for controlling the display of information on a suitable display 132 (see paragraph [0026] and FIG.1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to combine Lee et al.'s apparatus in FIG.10-11 with the teachings of Lee et al.'s apparatus in FIG.3, Findakly et al. and Sheaffer for using a converter that converts the electrical response signals from the memory devices to the optical signals which couples to the T/R unit 148 for communicating with the controller, implementing the characteristics of reflectances of the partial reflectors in the beam splitters 870a-d of Lee et al. through the common optical bus and using graphic controller which connects to the memory controller for controlling the display of information on a display because it would allow the memory controller system achieving fewer signal power loss along the optical path to the memory controller by applying optical communication technique, receiving the equal amount of optical power signal at the associated optical receiver and the optically-coupled memory system having

accurate and useful display system for displaying the receiving data signals from the memory devices.

Regarding to claim 26, Lee et al., Findakly et al. and Sheaffer disclose everything claimed as applied above (see claim 25). In addition, Lee et al. disclose the apparatus further includes: wherein the integrated circuit is a memory controller (controller 850) (see paragraph [0042] lines 1-4 and FIG.10).

Regarding to claim 27, Lee et al., Findakly et al. and Sheaffer disclose everything claimed as applied above (see claim 25). In addition, Lee et al. disclose the apparatus further includes: wherein the integrated circuit is a processor (see paragraph [0042] lines 1-4 and FIG.10 where in a processor inherently exists inside the controller 850).

Response to Arguments

4. Applicant's arguments filed on 01/23/2008 with respect to claims 1-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHYOWAI LIN whose telephone number is (571)270-1659. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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PWL 05/07/2008

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